Processor With Annul Under Mask Technology For Improved Branch Efficiency

Sub B1

ABSTRACT OF THE DISCLOSURE

A processor (50) having a changeable architected state. The processor includes an instruction memory (52) for storing instructions. The processor also includes an instruction pipeline, where an instruction which passes entirely through the pipeline alters the architected state. Further, the pipeline comprises circuitry for fetching (58aa) instructions from the instruction memory into the pipeline. The processor also includes circuitry for storing an annul code (46) corresponding to instructions in the pipeline. Finally, the processor includes circuitry for preventing (FU_1 through FU_8) one or more selected instructions in the group from altering the architected state in response to the annul code.